Amendments to the Specification:

Please change the title to --METHOD OF MANUFACTURING A SEMICONDUCTOR PACKAGE--.

Please replace the paragraph extending from Page 1, line 10 to line 16, with the following rewritten paragraph:

The present application is a continuation-in-part of U.S. Patent Application "INTEGRATED CIRCUIT SUBSTRATE HAVING LASER-EMBEDDED CONDUCTIVE PATTERNS AND METHOD THEREFOR", Serial number 10/138,225 filed on May 1st, 2002, now U.S. Patent No. 6,930,256, issued August 16, 2005, by at least one common inventor and assigned to the same assignee. The specification of the above-referenced Patent Application is herein incorporated by reference.

Please replace the paragraph extending from Page 3, line 3 to line 10, with the following rewritten paragraph:

Also, when combining multiple semiconductor packages in an assembly, at times it is advantageous to permit removal ~~or~~ of at least of one semiconductor package, so that when one semiconductor package is used with one of multiple alternative other semiconductor packages in a three-dimensional configuration, the interconnect between a semiconductor package may be standardized and so that one of the semiconductor packages may be removed and replaced without removing the other.

Please replace the paragraph extending from Page 5, line 1 to line 3, with the following rewritten paragraphs:

Figure 1C is a pictorial diagram depicting a cross sectional side view of the semiconductor package of Figure 1B after vias are filled;

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Figure 1D is a pictorial diagram depicting a cross sectional side view of the semiconductor package of Figure 1C after solder balls are attached to lands;

Please replace the paragraph extending from Page 10, line 16 to page 11, line 4, with the following rewritten paragraph:

Referring now to Figure 2C, an electronic assembly 50 is shown in accordance with another embodiment of the invention. Vias 54 are provided through to electrical connections 53 of die ~~41~~ 51, providing a direct interface from the circuits of die 51 to circuits within piggybacked semiconductor die 56, which is depicted as a flip-chip die. Attachment of semiconductor die 56 is made via solder balls 58 (or alternatively posts) where semiconductor die 56 is custom package layout designed to interface with electrical connections 53 of die 51. The depicted configuration is especially useful where die 56 is one of several interchangeable dies that may be used to upgrade or provide options for use with die ~~53~~ 51. An optional encapsulation 57, is depicted as deposited over die 56.

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